In the Claims:

Claim 1 (original): A memory cell structure comprising:

a semiconductor substrate;

a first silicon oxide layer situated over said semiconductor substrate;

a charge storing layer situated over said first silicon oxide layer, said charge storing layer comprising silicon nitride having reduced hydrogen content, said reduced hydrogen content reducing charge loss in said charge storing layer;

a second silicon oxide layer situated over said charge storing layer;

a gate layer situated over said second silicon oxide layer.

Claim 2 (original): The memory cell structure of claim 1, further comprising:

said first silicon oxide layer, said charge storing layer, said second silicon oxide layer, and said gate layer forming a gate stack, said gate stack having a sidewall;

a spacer adjacent to said sidewall of said gate stack, said spacer comprising silicon nitride having reduced hydrogen content, said reduced hydrogen content reducing charge loss in said charge storing layer.

Claim 3 (original): The memory cell structure of claim 2, wherein said gate stack is situated over a channel region in said semiconductor substrate, said channel region situated between a first terminal region and a second terminal region.

Claim 4 (original): The memory cell structure of claim 1, wherein said charge storing layer has a hydrogen content less than 1.0 atomic percent.

Claim 5 (original): The memory cell structure of claim 1, wherein said charge storing layer has a hydrogen content between 0 and 0.5 atomic percent.

Claim 6 (original): The memory cell structure of claim 1, wherein said charge storing layer is capable of storing two bits.

Claim 7 (original): The memory cell structure of claim 1, wherein said charge storing layer is formed from nitrogen radicals.

Claims 8-13 (canceled).

Claim 14 (original): A memory cell structure comprising:

a semiconductor substrate, a first silicon oxide layer situated over said semiconductor substrate, a charge storing layer situated over said first silicon oxide layer, a second silicon oxide layer situated over said charge storing layer, a gate layer situated over said second silicon oxide layer, said memory cell structure characterized by:

said charge storing layer comprising silicon nitride having reduced hydrogen content:

said reduced hydrogen content reducing charge loss in said charge storing layer.

Claim 15 (original): The memory cell structure of claim 14, further comprising:

said first silicon oxide layer, said charge storing layer, said second silicon oxide layer, and said gate layer forming a gate stack, said gate stack having a sidewall;

a spacer adjacent to said sidewall of said gate stack, said spacer comprising silicon nitride having reduced hydrogen content, said reduced hydrogen content reducing charge loss in said charge storing layer.

Claim 16 (original): The memory cell structure of claim 14, wherein said gate stack is situated over a channel region in said semiconductor substrate, said channel region situated between a first terminal region and a second terminal region.

Claim 17 (original): The memory cell structure of claim 14, wherein said charge storing layer has a hydrogen content less than 1.0 atomic percent.

Claim 18 (original): The memory cell structure of claim 14, wherein said charge storing layer has a hydrogen content between 0 to 0.5 atomic percent.

Claim 19 (original): The memory cell structure of claim 14, wherein said charge storing layer is capable of storing two bits.

Claim 20 (original): The memory cell structure of claim 14, wherein said charge storing layer is formed from nitrogen radicals.